What is claimed is:

1. A method for fabricating a ferroelectric memory device, comprising the steps of:

forming a first insulation layer on a substrate;

forming a storage node contact contacting to a partial portion of the substrate by passing through the first insulation layer;

forming a stack pattern of a lower electrode contacting to the storage node contact and a hard mask on the first insulation layer;

forming a second insulation layer on an entire surface of the resulting structure including the stack pattern;

planarizing the second insulation layer until a surface of the hard mask is exposed;

removing selectively the exposed hard mask to make a surface level of the lower electrode lower than that of the second insulation layer; and

forming sequentially a ferroelectric layer and an upper electrode on the second insulation layer and the lower electrode.

2. The method as recited in claim 1, wherein the hard mask is made of titanium nitride, tantalum nitride or silicon oxide.

3. The method as recited in claim 1, wherein the step of

making the surface level of the lower electrode lower than that of the second insulation layer proceeds by performing a wet etching process or a dry etching process to the hard mask.

4. The method as recited in claim 3, wherein the wet etching process uses one of cleaning agents such as SC-1 comprising ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and water (H_2O) in a ratio of about 1 to about 4 to about 20 and SPM comprising sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in a ratio of about 4 to about 1.

5. The method as recited in claim 3, wherein the dry etching process uses a mixed gas of argon (Ar) and chlorine (Cl).

6. The method as recited in claim 1, wherein the step of planarizing the second insulation layer until the surface of the hard mask is exposed includes the steps of:

planarizing a partial portion of the second insulation layer by performing a chemical mechanical polishing (CMP) process; and

performing an etch-back process to the second insulation layer to make the hard mask exposed.

7. The method as recited in claim 1, wherein the step of planarizing the second insulation layer until the surface of the hard mask is exposed proceeds by applying a CMP process or

an etch-back process at once to the second insulation layer.